17.1 An SOI-Based 7.5µm-Thick 0.15×0.15mm² RFID Chip

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Radio frequency identification (RFID) technology [1] is expected to provide a "bridge" of information between the real world and the virtual world of the Internet. For this to be possible, the cost of manufacture of RFID devices should be reduced and the mechanical stress endurance increased. Thinner chips are also needed if RFID tags are to be attached to paper media and other small goods. The use of silicon on insulator (SOI)-based CMOS [2] has made possible small RFID chips measuring 0.15mm×0.15mm×7.5µm. Moreover, the use of a double-surface electrode [3] on an ultra-thin RFID chip has eased the difficulty of handling small chips and has reduced the cost of attaching RFID antennae.

Figure 17.1.1 shows the field-powered RFID chip circuit developed for the identification memory. It consists of a 128b ROM, which is programmed during wafer processing. The output of the ROM controls the impedance of the power rectifier circuit. The RFID reader identifies data from the RFID chip by detecting the back-scattering level of radiation power emitted from the reader. The power rectifier circuit generates a Vdd voltage from the received 2.45GHz carrier-frequency energy and supplies the voltage to the ROM and its control circuit. The clock envelopment circuit, which has the same circuit scheme as the power rectifier circuit except for the load capacitance, envelops the clock signal on the carrier wave with a 100kHz clock. The front-end of this chip has been designed with a 0.18µm SOI CMOS process. The input from the antenna to each circuit is directly connected to a capacitor designed with a varactor device structure using an N-well. The full-swing input signal from the antenna terminal is rectified by a capacitor and diode combination circuit.

Figure 17.1.2 compares the front-end device structure of the SOI CMOS device with a conventional device. The input signal level may reach 2V or higher when the RFID chip is close to the reader antenna. Therefore, the conventional device needs a two-way or three-way guard ring structure to prevent latch-up from occurring between the well and the substrate. In contrast, in the SOI device, the capacitor and diode devices are insulated by oxide, which enables the RF devices of the chip to be tightly laid out. In the conventional capacitor, the input from the antenna can not be directly connected to the N-well of the device in order to prevent latch-up, and hence the varactor device structure can not be efficient. SOI CMOS, however, can employ a capacitor structure that is ideal for making a small device. Moreover, the SOI parasitic capacitance between the N-well of the capacitor and the substrate is very small, reducing dynamic leakage current. Lowering the forward voltage drop of the diode is an effective way to increase the efficiency of the rectifier circuit. Therefore, the active body contact technology of SOI CMOS can reduce the forward voltage without special devices such as a Schottky diode.

Figure 17.1.3 shows the ROM circuit of the RFID chip. The memory cell consists of one transistor and a wire-connection ROM program position. Each transistor is commonly wired at the drain line, of which parasitic capacitance is used to hold electrons. The precharge and discharge memory control timing is conducted with a 10b control register. This memory scheme is simple and dissipates very little power. The simplified wire-connection ROM architecture can operate over a wide temperature range (-196˚C to 350˚C). These characteristics seem to be suitable for ubiquitous applications.

Ultra-thin RFID chips are easily realized by using SOI wafers. Figure 17.1.4 shows the ultra-thin chip fabrication process and double-surface electrode structure, which can be described in four steps. Step1: The device is fabricated on an SOI wafer. The top electrode of each device is formed at the surface of the wafer by using gold plating or a sputtering technique. Step 2: The finished wafer is placed upside-down on a support sheet and the substrate of the wafer is thinned by means of back grinding and back drying or wet etching. The buried oxide layer of the SOI wafer is useful as an etch stop. Step 3: The back electrode is formed on the back surface. The connection path to the active RFID device is made by making a via hole through the buried oxide layer. To separate the chips, a narrow pattern is etched on the surface metallization. Step 4: The chip separation is accomplished by dry etching with the back electrode pattern as an etching mask. The narrow etching width of 5µm-10µm helps to increase the chip yield of the wafer. Moreover, silicon chipping-less separation helps to improve the mechanical stress endurance of the chip. The double-surface electrode technique becomes more useful as the RFID chip gets smaller. The small ultra-thin chip can be mounted on the RFID antenna without worrying about the chip's orientation with respect to the antenna. This mounting flexibility makes it possible to mount many chips onto many antennae, which significantly reduces the RFID assembly cost.

Figure 17.1.5 shows part of a cross-section of the antenna connection to the chip. A thin anisotropic conductive film (ACF) connection technique was used to fabricate the RFID inlet, which is thinner than 50µm, for versatile individual recognition applications with thin media such as paper. Here, the inlet holds the intermediate fabrication unit of the device, which consists of the chip and its antenna.

Figure 17.1.6 shows reader detection signal level as a function of communication distance. The back-scattered signal from the RFID device is branched to the detection circuit via a circulator at the front-end of the reader. The maximum communication distance is 480mm, given a reader output power of 300mW and a reader antenna gain of 11dBi. The phase difference between the I-signal and Q-signal is 90 degrees.

Figure 17.1.7 is a micrograph of the developed chip with the surface electrode pattern removed. This chip was designed with four metallization levels, with the upper metal dedicated to focused-ion beam (FIB) modifications. There were up to 26 FIB modification design points, and these were used to evaluate the RF circuit characteristics of this chip

Acknowledgements:
The authors would like to express special appreciation to Y. Nakase, Y. Takebe and Y. Okada for laying out this chip circuit and would like to thank K. Ito, A. Maeda, K. Ootsuka, T. Ishige, T. Takasugi, O. Horiuchi, T. Sasaki, H. Ishizaka, K. Tasaki, H. Matsuzaka, N. Matuszaka, T. Satou, T. Naito, T. Furuya, A. Koide, H. Tomotsune, O. Watanabe, R. Imura, T. Kawaguchi, H. Kandou, and M. Ashizawa for their significant contributions to this work.

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[2] Y. Hirano et al., "Impact of 0.10µm SOI CMOS with body-tied hybrid trench isolation structure to break through the scaling crisis of silicon technology," IEDM Tech. Digest, pp. 467-470, Dec. 2000.
[3] S. Briole et al., "AC-Only RF ID Tags for Barcode Replacement," ISSCC Dig. Tech. Papers, pp. 438-439, Feb. 2004.

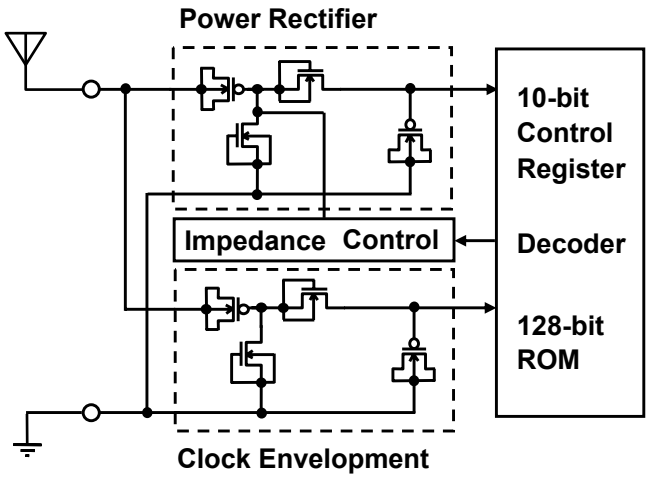

Figure 17.1.1: Circuit structure of ultra-thin small RFID chip.

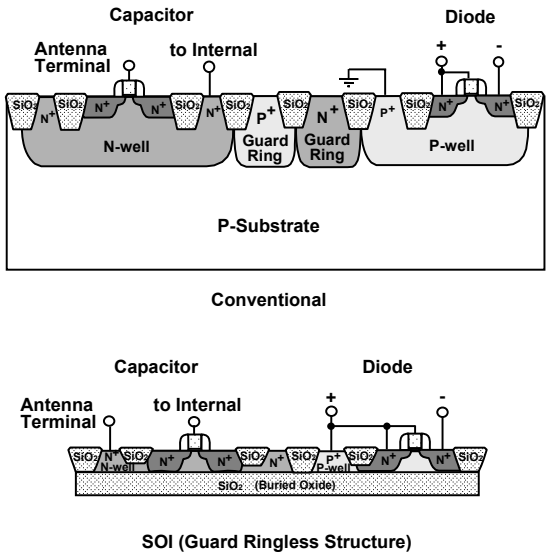

Figure 17.1.2: Comparison of RF front-end device structures.

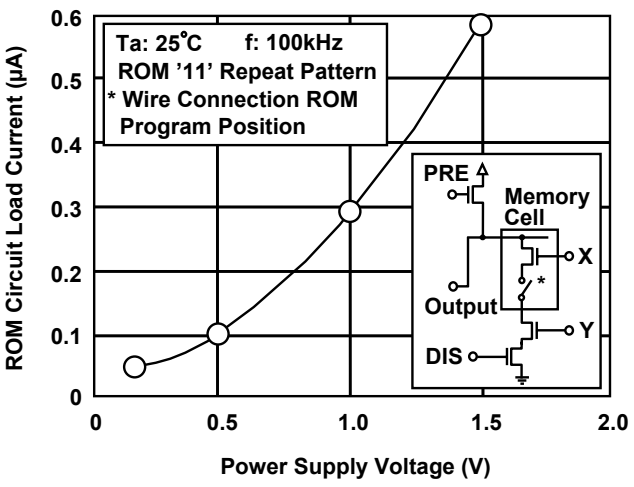

Figure 17.1.3: ROM circuit scheme and load current characteristics.

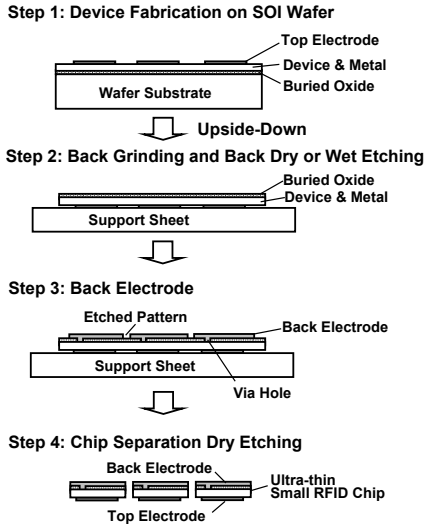

Figure 17.1.4: Ultra-thin chip fabrication process and double-surface electrode structure (cross section).

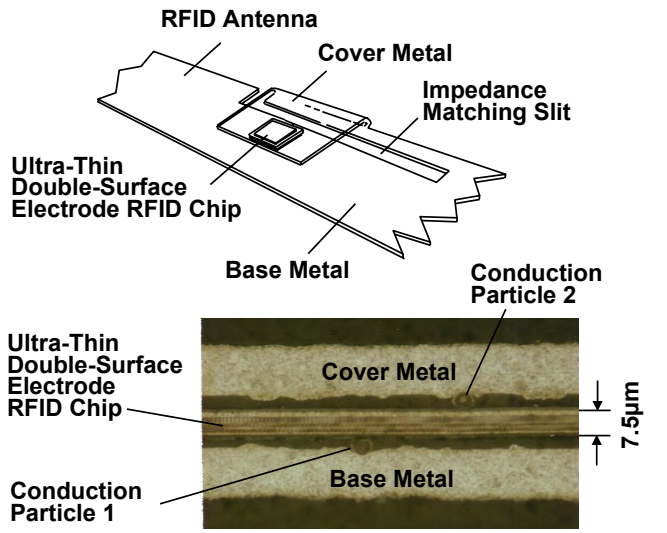

Figure 17.1.5: Partial cross section of antenna connection to ultra-thin double-surface electrode chip.

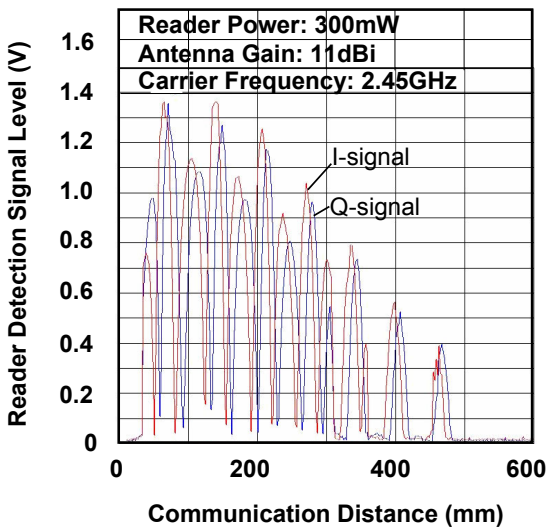

Figure 17.1.6: Reader detection signal level depending oncommunication distance.

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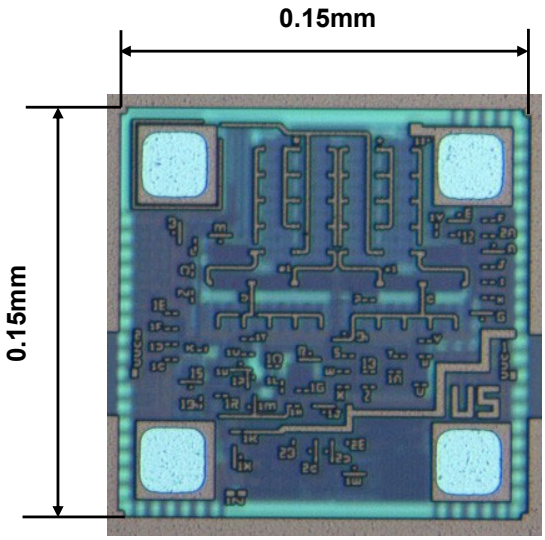

Figure 17.1.7: Micrograph of ultra-thin small RFID chip.

